

Notice of References Cited	Application/Control No. 10/043,237	Applicant(s)/Patent Under Reexamination DOUMAE, YASUHIRO	
	Examiner William C. Vesperman	Art Unit 2813	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,866,448	02-1999	Pradeep et al.	438/231
	B	US-5,409,848	04-1995	Han et al.	438/302
	C	US-2002/0068395	06-2002	Tran et al.	438/194
	D	US-6,352,885	03-2002	Wieczorek et al.	438/197
	E	US-6,087,706	07-2000	Dawson et al.	257/520
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	A Novel Self-aligned Gate-overlapped LDD Poly-Si TFT with High Reliability and Performance", published in the IEEE in 1977 and authored by Mutsuko Hatano, Hajime Akimoto and Takeshi Sakai.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.